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(54) Method for realizing a multilevel ROM memory in a dual gate CMOS process and corresponding ROM memory cell

(57) The invention relates to a method of producing a multi-level memory of the ROM type in a CMOS process of the dual gate type, which method comprises at least the following steps:

on a semiconductor substrate, defining respective active areas for transistors of ROM cells (1), electrically erasable non-volatile memory cells, and low- and high-voltage transistors;

depositing a layer of gate oxide over said active areas;

depositing a polysilicon layer over the gate oxide layer;

masking, and then etching, the polysilicon layer to define, by successive steps, respective gate regions of the ROM cells, non-volatile cells, and low- and high-voltage transistors;
characterized in that it further comprises the following steps:

masking the polysilicon layer (4) of some of the transistors of the ROM cells (1), and implanting a first dopant species (N) in the active areas (2) of the exposed transistors;

removing the mask from the polysilicon layer (4), and implanting a second dopant species (P) in said previously covered layer;

masking and subsequently etching the polysilicon layer to define the gate regions of the ROM cell transistors.

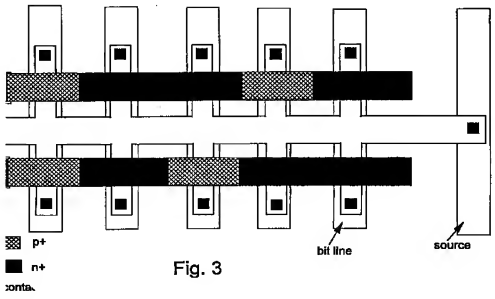

Fig. 3

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Description

Field of the Invention

[0001] This invention relates to a method of producing a multi-level memory of the ROM type in a CMOS process of the so-called dual gate type, and to a memory cell structure produced thereby.

[0002] In particular, the invention relates to a method as above which comprises at least the following steps:

on a semiconductor substrate, defining respective active areas for transistors of ROM cells (1), electrically erasable non-volatile memory cells, and low- and high-voltage transistors;

depositing a layer of gate oxide over said active areas;

depositing a polysilicon layer over the gate oxide layer;

masking, and then etching, the polysilicon layer to define, by successive steps, respective gate regions of the ROM cells, non-volatile cells, and low- and high-voltage transistors.

[0003] The invention also relates to a ROM structure, with transistor cells integrated in a semiconductor by a dual gate CMOS process along with electrically erasable non-volatile memory cells and low- and high-voltage transistors; all the cells and transistors having active areas covered with a layer of gate oxide, in turn overlaid by a polysilicon layer.

[0004] As is well known in this specific technical field, there exists a growing demand from the market for integration, in a single semiconductor electronic device, of both ROM (Read Only Memory) circuits and non-volatile, but electrically erasable, memories such as EEPROMs and/or Flash EEPROMs. Filling this demand, which is more pressing from the smart card market, calls for significant complications in the manufacturing process of such integrated electronic devices.

[0005] The technologies involved in providing either circuit types are not fully compatible, in fact. Accordingly, production costs become higher, and achieving high yield rates is made more difficult.

[0006] In addition, continuing advances in criptographic techniques exact the use of codes of increasing size in terms of number of bits which are not easily decrypted by reverse engineering methods.

[0007] It is also recognized that an array of ROM cells is essentially an array of MOS transistors having conventional source, drain, and gate terminals, and threshold voltages which are set during their fabrication process.

[0008] The threshold is also differentiated such that, for any given bias of the transistor gate terminal, it becomes possible to determine which cells are in the 'on' (logic 1) state and which are instead in the 'off' (logic 0) state by means of a suitable sensing circuit. Telling which cells are in the logic 1 state and which in the logic 0 state is usually achieved by implanting or not implanting the source and drain junctions during the step of implanting these transistor regions.

[0009] This prior approach provides cells with a logic value of 1 and/or 0, without a preliminary optical analysis enabling them to be discerned.

[0010] Other approaches allow the logic value of 1 or 0 to be determined based on the presence or absence of a transistor.

[0011] In either cases, there is no current technology available which can provide a multi-level ROM structure, that is, a structure which can store several logic values in each memory cell.

[0012] The underlying technical problem of this invention is, therefore, to provide a novel method of producing a multi-level type of ROM in a CMOS process of the dual gate type, expanding the information storage capacity by means of a readily integratable component with CMOS technology.

Summary of the Invention

[0013] The concept behind this invention is one of providing a ROM type of memory cell which can store at least three discrete logic levels. Such a cell is obtained by two different dopings of the polysilicon layer that forms the gate region of the transistor.

[0014] The step of implanting the source/drain regions of the transistor which comprises the cell is, therefore, substantially separated from the polysilicon implanting step.

[0015] Based on this concept, the technical problem is solved by a method as previously indicated and defined in Claim 1 foll..

[0016] The technical problem is also solved by a memory cell structure as defined in Claim 4.

[0017] The features and advantages of the method and memory cell structure according to the invention will become apparent on reading the following description of embodiments thereof, given by way of non-limitative examples with reference to the accompanying drawings.

Brief Description of the Drawings

[0018]

Figure 1 is an enlarged view from above illustrating schematically a portion of a semiconductor integrated circuit which incorporates at least one ROM cell formed in accordance with this invention.

Figure 2 is an enlarged view from above illustrating schematically the same portion of an integrated cir-

cuit during a subsequent step of the inventive method.

Figure 3 is an enlarged view from above illustrating schematically the same portion of an integrated circuit during a further subsequent step of the inventive method.

Detailed Description

[0019] The process steps and structures described herein below do not reflect a complete process flow for manufacturing integrated circuits. The present invention can be practiced in combination with state-of-art techniques as currently employed in the manufacture of integrated circuits, and only such commonly used process steps will be discussed as are necessary for understanding the invention.

[0020] The drawing figures which show cross-sections taken through portions of an integrated circuit during its fabrication are not drawn to scale, but rather drawn as appropriate to highlight major features of the invention.

[0021] Referring in particular to Figure 1, those steps of the method of this invention which lead to forming multi-level ROM cells in a CMOS process of the dual gate type will now be described.

[0022] In CMOS processes of the latest generation, MOS transistors are usually formed with their gate regions doped with the same dopant type as the channel region, and it is to this feature that the term "dual gate" applies in technical language. To this aim, it is necessary for the gate region to be left unprotected during the process step which provides heavy source drain implants.

[0023] Advantageously in this invention, the memory circuit that incorporates the ROM cells 1 is integrated in a semiconductor together with a memory circuit of a different type incorporating electrically erasable non-volatile cells of the EEPROM or Flash EEPROM type. Circuitry is also associated with the matrix of memory cells which includes both low-voltage (LV) MOS transistors and high-voltage (HV) MOS transistors.

[0024] The source and drain junctions of low-voltage MOS transistors are usually formed with a gentle profile by a double dopant implantation referred to as LDD (Lightly Doped Drain) implantation.

[0025] In the integrated memory circuit of this invention, the HV transistors are needed for handling high (>12V) voltages during the step of programming the non-volatile memory cells.

[0026] During the heavy source and drain implanting step applied to the LV transistors, the HV transistors are wholly masked off. The heavy implantation is only carried out in contact regions, to ensure good contacting.

[0027] The effectuation of those steps which are involved in the inventive method will now be described.

[0028] Reference will be made to an instance of the memory cells being N-channel cells, although the same considerations would also apply to P-channel cells once all dopant types are reversed.

[0029] First defined on a semiconductor substrate 10 are the active areas of the various transistors which comprise the memory circuits described hereinabove. Thus, both the active areas of the ROM cells 1 and the active area of the non-volatile memory cells forming the Flash EEPROM circuit portion are defined. In addition, low- and high-voltage MOS transistors of the circuitry associated with the cell matrix are formed.

[0030] For example, active areas 2 are defined for the transistors of the ROM cells, as shown in Figure 1. Of course, there would be one transistor for each active area.

[0031] The active areas 2 are T-shaped. Shown in Figure 1 are an arbitrary number of adjacent cells, each having a respective active area 2.

[0032] Grown on top of the active areas 2 is a thin layer 3 of gate oxide. This step implies oxidation of the whole memory circuitry.

[0033] At this stage, a layer 4 of polysilicon, as required for forming the gate regions of the memory cell transistors, is deposited.

[0034] Conventional masking, etching, flushing, and implanting steps enable definition of the standard low-voltage MOS transistors with source and drain junctions of the LDD type. These steps lead to the definition of the poly layer, and are preliminary to the LDD light implanting steps, formation of spacers, and heavy source and drain implantations, also for the LDD transistors.

[0035] However, the gate regions of the ROM cell transistors are defined at a later stage, and so are those of the EEPROM cells and the HV transistors.

[0036] During the source and drain n+ implanting step for the low-voltage transistors, certain ROM cells 1, such as those referenced 5 in Figure 2, are masked such that their gate region layer of polysilicon can be subjected to a subsequent p+ dopant implanting step. This masking step essentially allows the logic state of the ROM cell to be programmed, and the mask can be regarded here as a program mask.

[0037] The above cells 5 will be exposed when the source and drain p+ implantation is to be carried out, whereas the previously implanted cells with N+ dopant will be covered.

[0038] In essence, one step of the inventive method provides for the poly layer 4 to be doped with N dopant, and a subsequent step provides for the same poly layer 4 to be doped with P dopant. During these implanting steps, the source and drain regions of the ROM cells 1 would be covered with the poly layer 4 and not implanted.

[0039] Thus, in the process of this invention, two separate different dopings are provided for the poly layer, which means that the process is a dual gate type wherein the gate is doped with the same dopant as the channel region of the cell.

[0040] Furthermore, it is important to have the

source/drain implantation separated in time from the polysilicon implantation.

[0041] At the end of these process steps, the polysilicon layer 4 of the matrix of ROM cells 1 will be doped in some areas with dopant of the N type, and in other areas with dopant of the P type. Accordingly, the poly layer 4 of the matrix of cells 1 with N-doped gates will exhibit a typical threshold, whereas the cells with P-doped gates will have a much higher threshold because of the different duty function of the P-doped polysilicon from the N-doped polysilicon. This enables the first two duty logic levels of the inventive memory structure to be defined.

[0042] With an appropriate masking step and subsequent etching, the poly layer of the matrix of cells 1 is then defined. By this etching, the HV transistors of the integrated circuit and the LV transistors forming the Flash EEPROM cells are also defined.

[0043] Further light source and drain implantations are provided for the matrix of ROM cells 1. During these implantations, a third logic level can be obtained by fully covering some cells, which will thus remain disconnected and carry no current under any bias conditions.

[0044] The solution proposed in this invention allows ROM cells to be produced with three logic levels each, in a dual gate process involving no more masks than are used in a standard process for making EEPROMs or Flash EEPROMs for smart cards.

[0045] The array of ROM cells is provided naturally with three logic levels per cell, which allows the information storage capacity of the ROM to be increased exponentially.

[0046] For example, with eight cells, this capacity is raised from 2^8 = 256 codes to 3^8 = 6,561 codes; with sixteen cells, it is raised from 65,536 codes to 43,046,721 different codes; etc..

[0047] It matters to observe that the ROM cells are produced according to the invention by differentially doping the gates of the corresponding transistors, also in a dual gate process environment.

[0048] Of course, the memory structure of this invention would require dedicated sensing circuitry for decrypting the logic information contained at the three levels of each cell by translating it from ternary to binary logics.

[0049] However, this represents no significant disadvantage when the increase in storage capacity is considered.

[0050] A further advantage of this three-level design is that ternary logics would make it even more difficult to grasp the information stored, viz. crypted, in the memory structure of this invention.

Claims

1. A method of producing a multi-level memory of the ROM type in a CMOS process of the dual gate type, comprising at least the following steps:

   on a semiconductor substrate, defining respective active areas for transistors of ROM cells (1), electrically erasable non-volatile memory cells, and low- and high-voltage transistors;

   depositing a layer of gate oxide over said active areas;

   depositing a polysilicon layer over the gate oxide layer;

   masking, and then etching, the polysilicon layer to define, by successive steps, respective gate regions of the ROM cells, non-volatile cells, and low- and high-voltage transistors;
   characterized in that it further comprises the following steps:

   masking the polysilicon layer (4) of some of the transistors of the ROM cells (1), and implanting a first dopant species (N) in the active areas (2) of the exposed transistors;

   removing the mask from the polysilicon layer (4), and implanting a second dopant species (P) in said previously covered layer;

   masking and subsequently etching the polysilicon layer to define the gate regions of the ROM cell transistors.

2. A method according to Claim 1, characterized in that, during the step of etching away the polysilicon layer to define the gate regions of the ROM cells (1), the gate regions of the high-voltage transistors are also defined.

3. A method according to Claim 1, characterized in that it comprises a light implanting step for the source and drain regions of the transistors of the ROM cells (1), and that during this implanting step some of the cells (1) are fully masked.

4. A ROM structure having transistor cells (1) integrated in a semiconductor by a dual gate CMOS process along with electrically erasable non-volatile memory cells and low-and high-voltage transistors, all cells and transistors having active areas covered with a layer of polysilicon, characterized in that some (5) of the cells have their polysilicon layer doped with a first type of dopant (N) and others have their polysilicon layer doped with a second type of dopant (P).

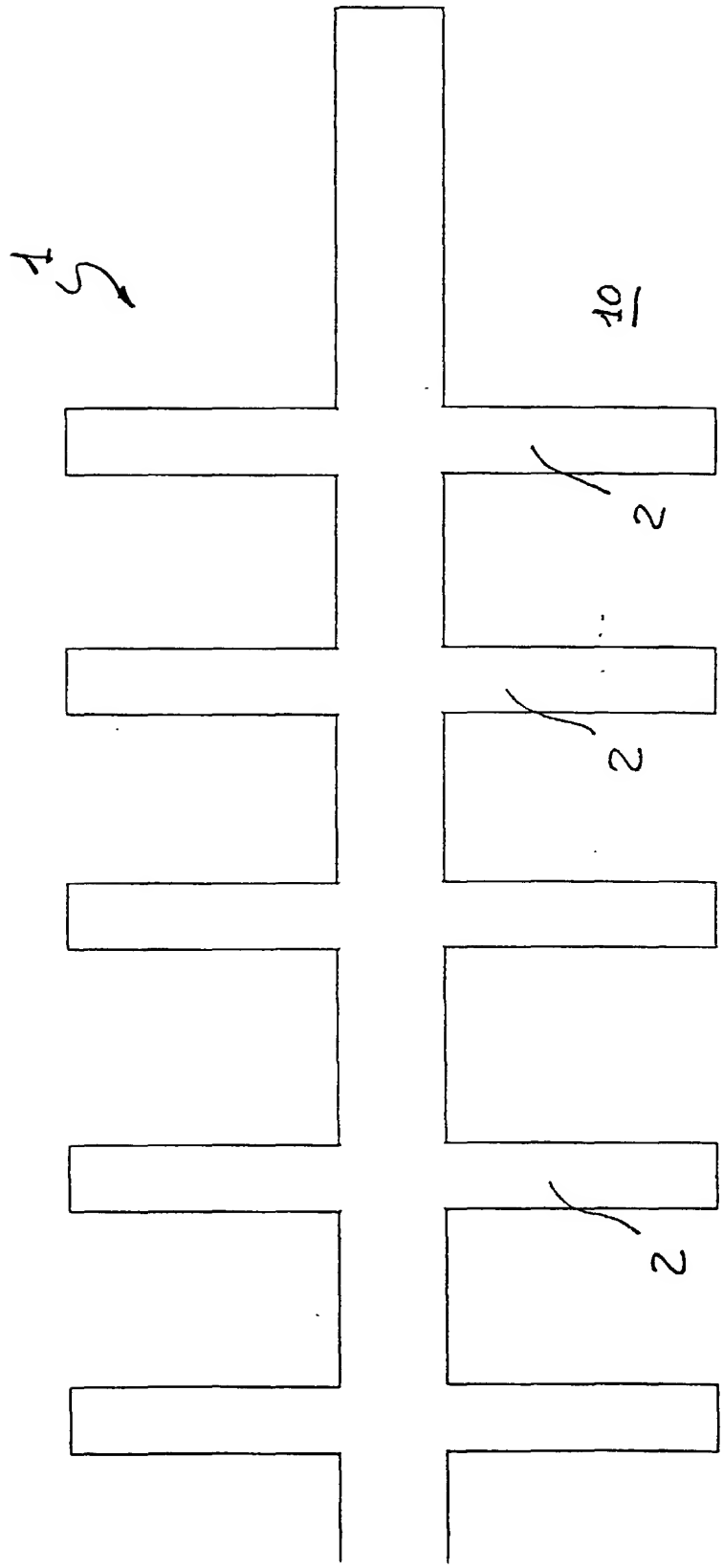

Fig. 1

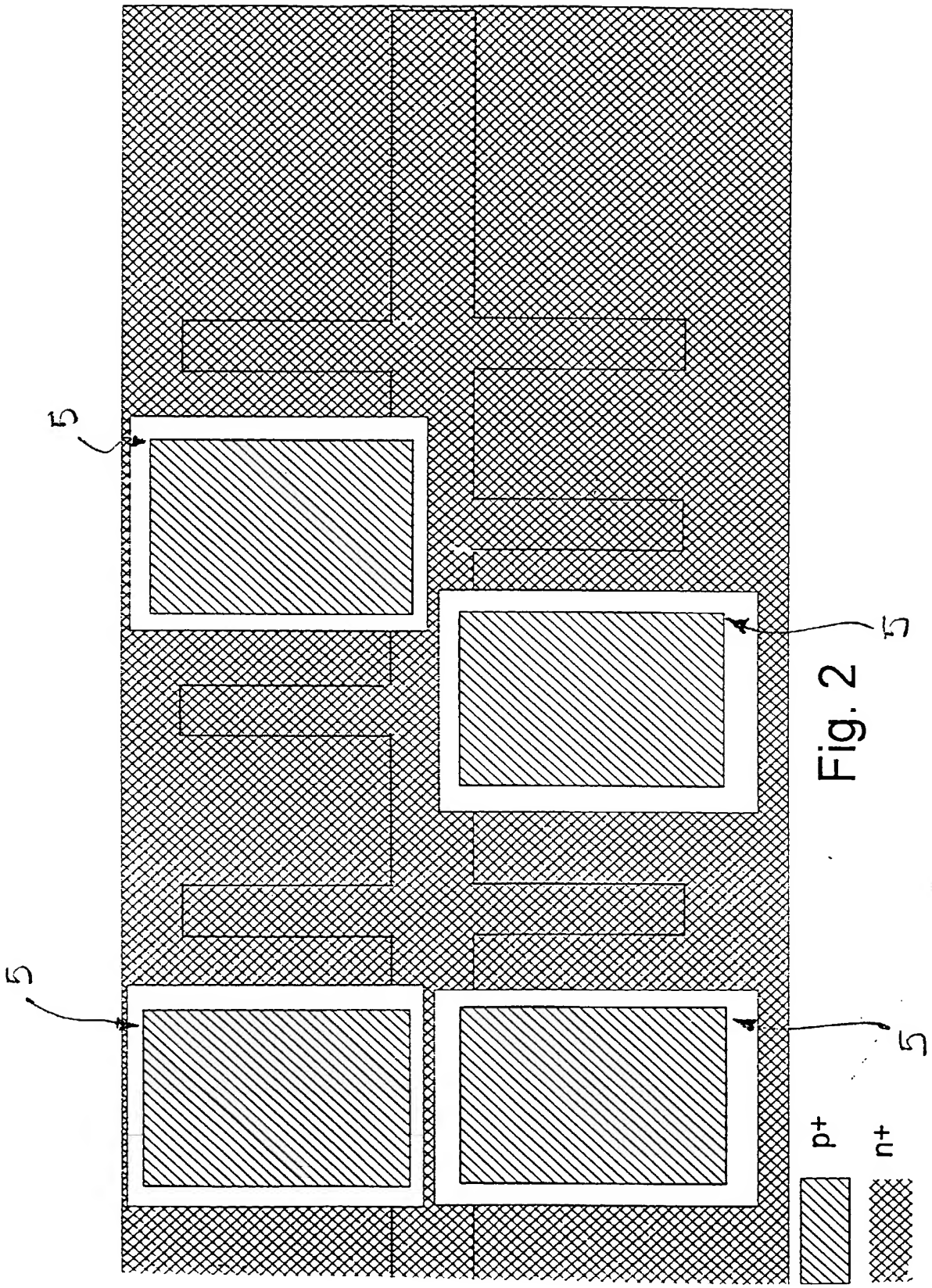

Fig. 2

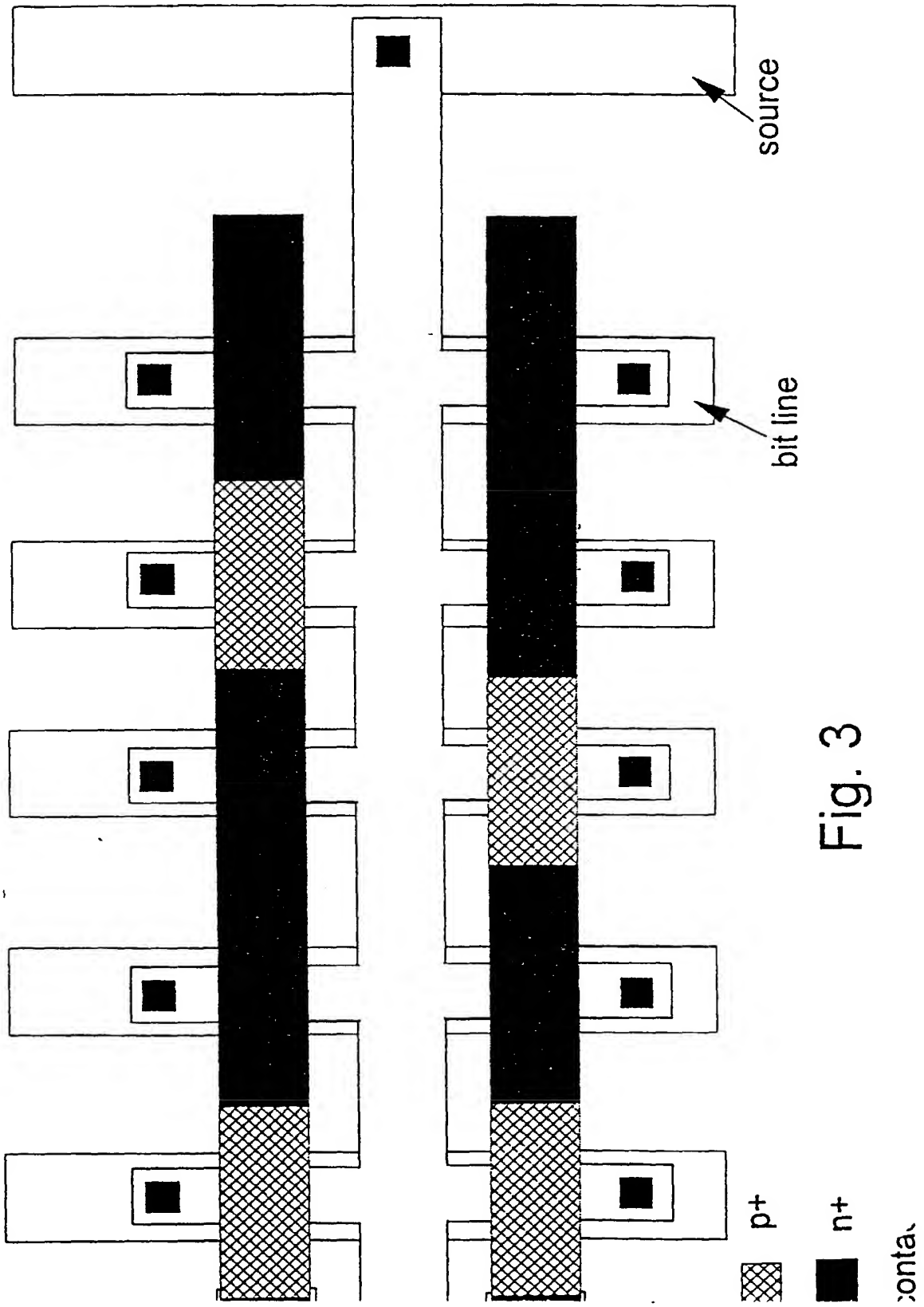

Fig. 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 83 0583

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 627 742 A (TOKYO SHIBAURA ELECTRIC CO) 7 December 1994 * abstract; figures 2,3,19-25 *	1-4	H01L21/8246 H01L27/112
A	US 5 504 030 A (CHUNG CHEN-HUI ET AL) 2 April 1996 * abstract; figures *	1-4	
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 423 (E-1127), 28 October 1991 & JP 03 177065 A (KAWASAKI STEEL CORP), 1 August 1991 * abstract *	1-4	
A	EP 0 661 751 A (TEXAS INSTRUMENTS INC) 5 July 1995 * abstract; figures *	1-4	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 April 1999	Wirner, C

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